

FIG. 1

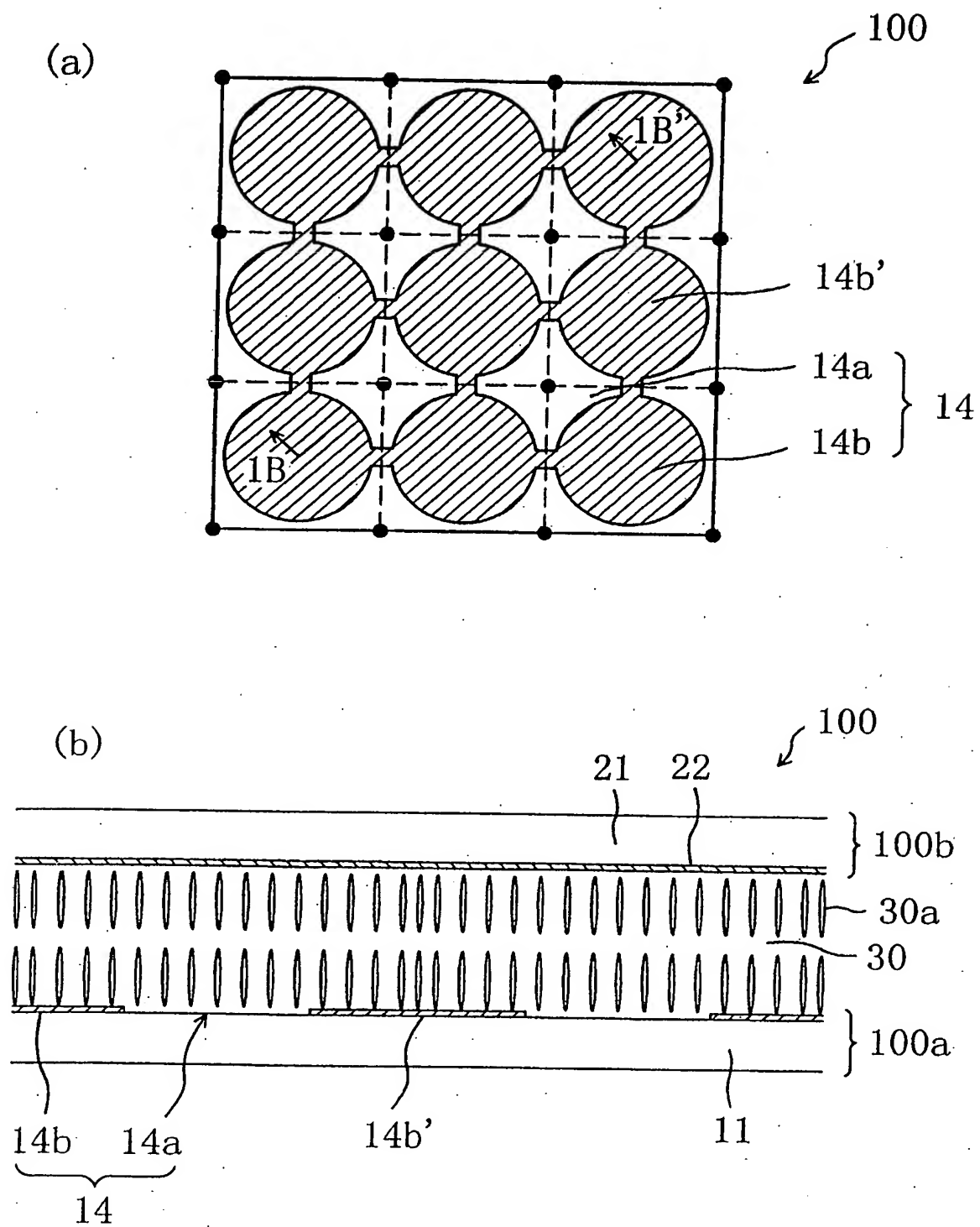


FIG. 2

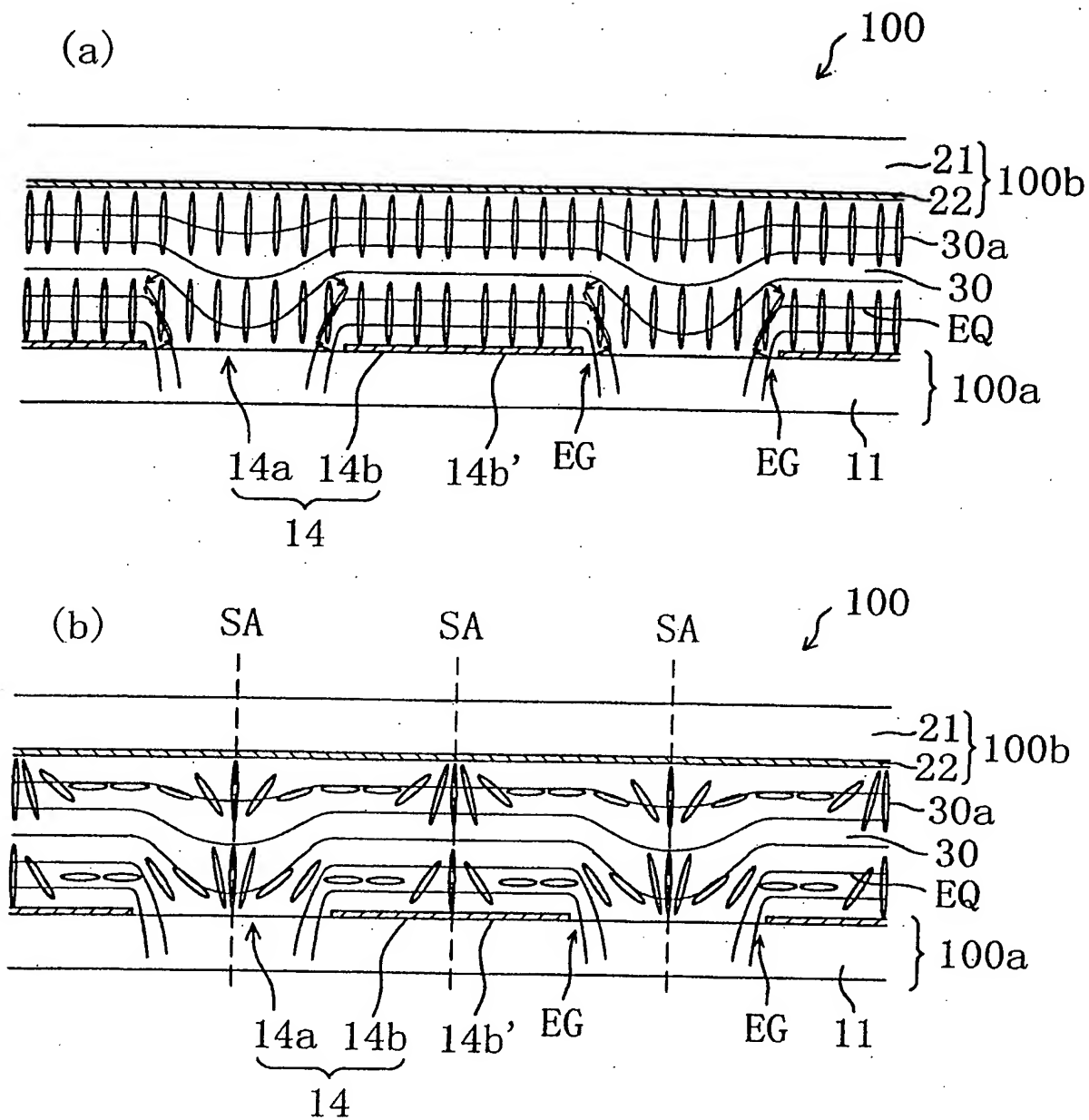


FIG. 3

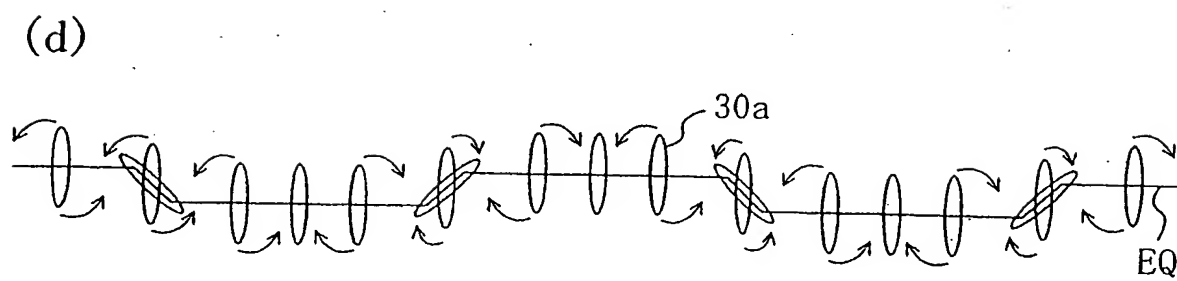
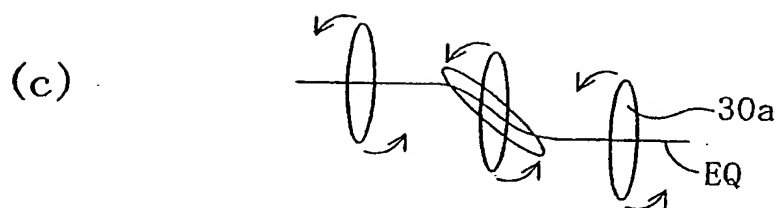
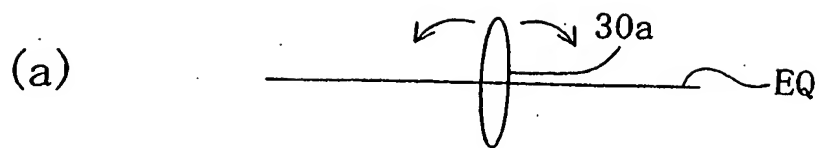
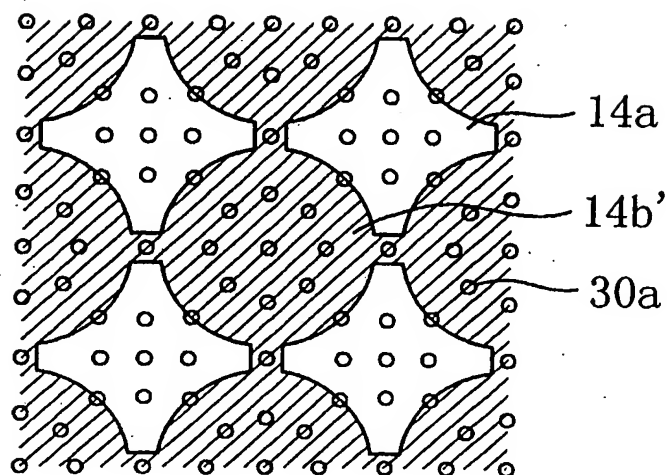
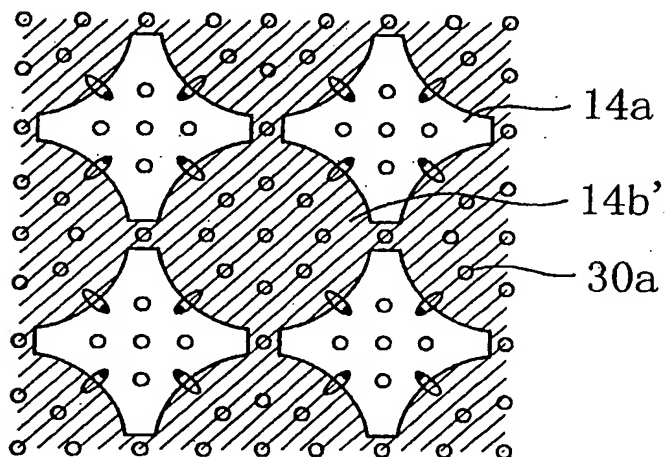


FIG. 4

(a)



(b)



(c)

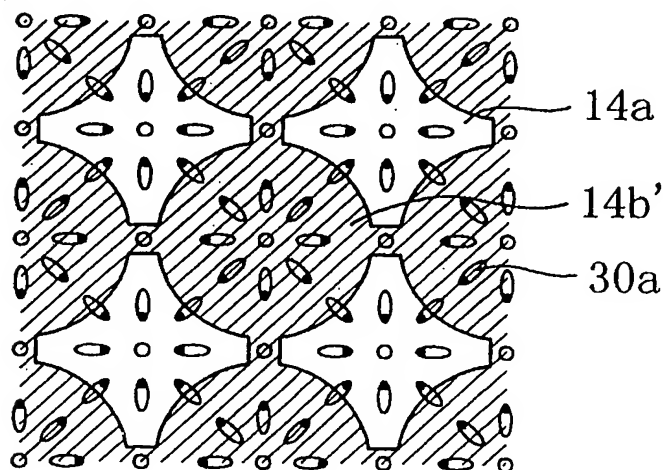


FIG. 5

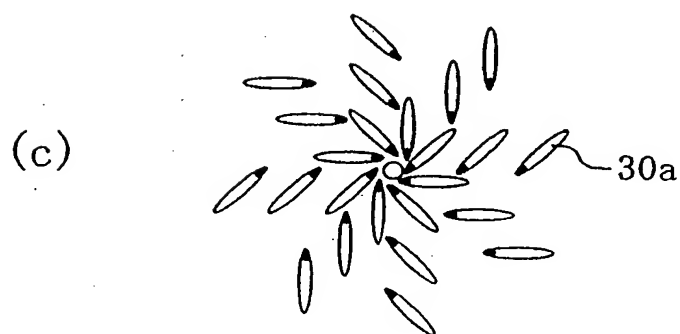
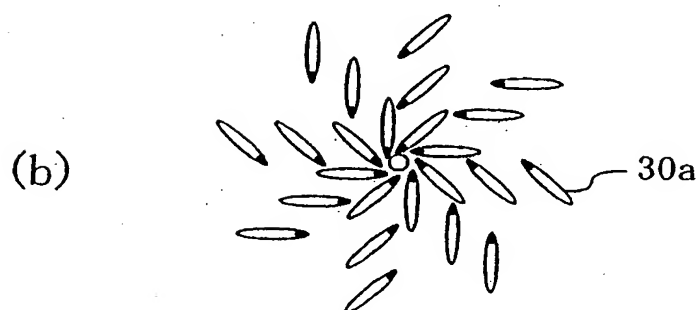
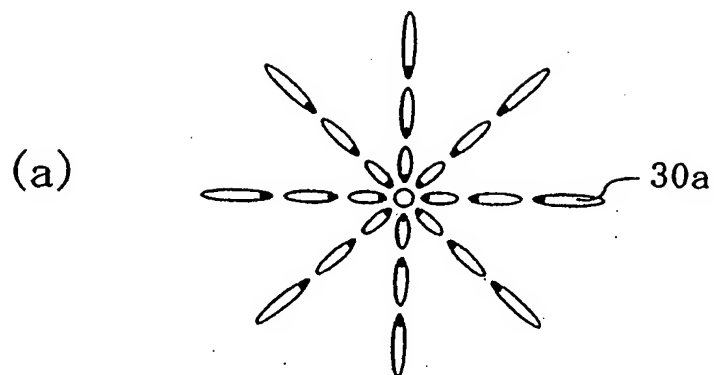


FIG. 6

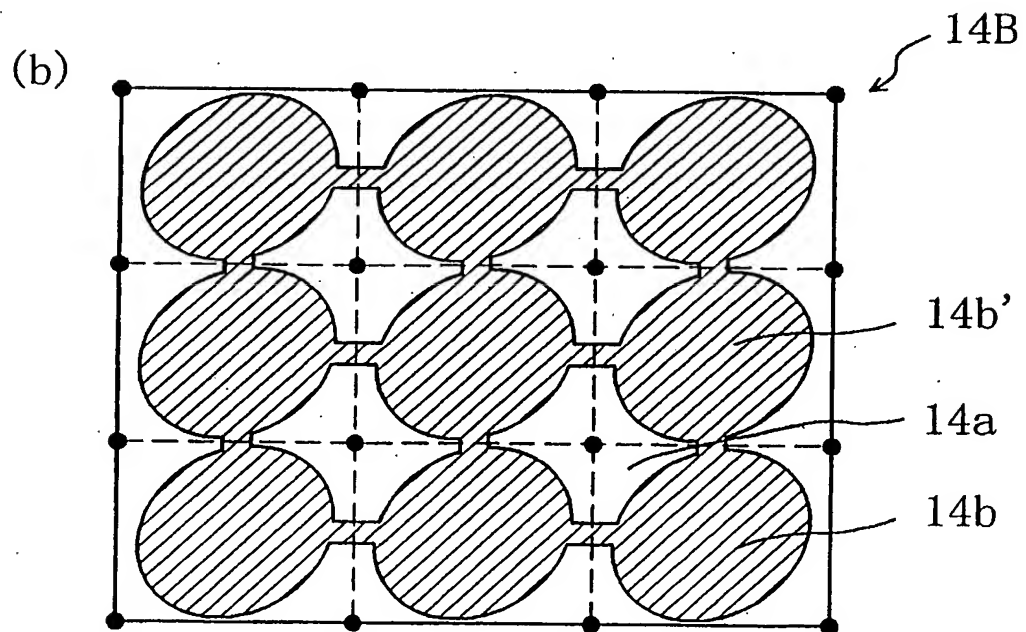
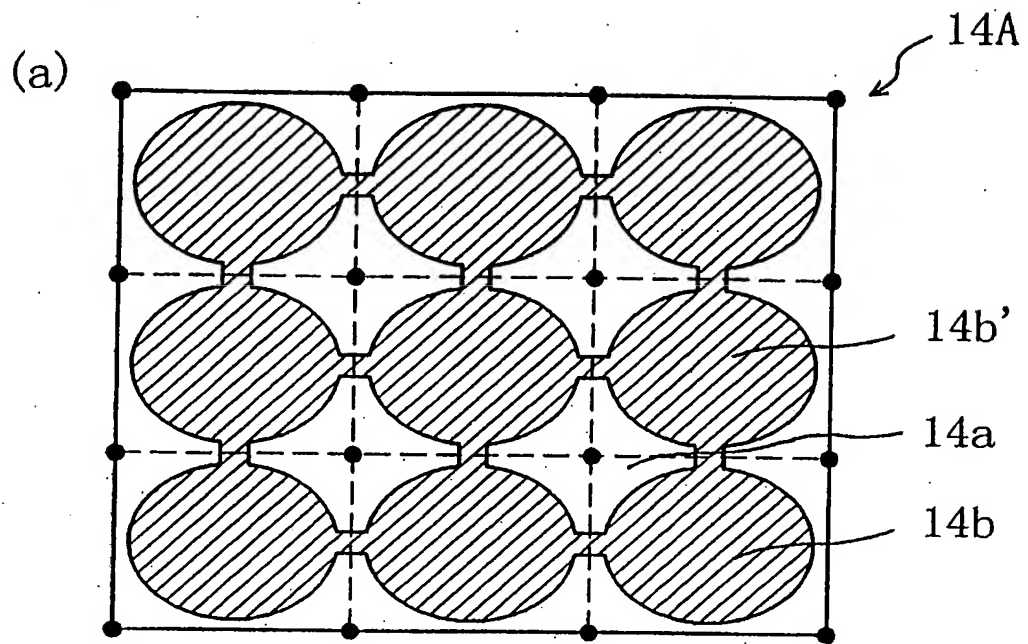
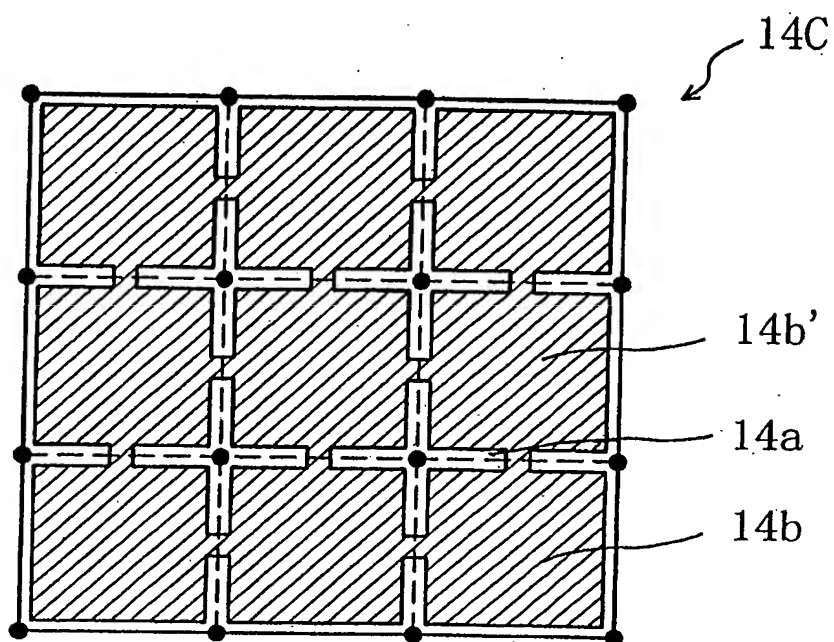


FIG. 7

(a)



(b)

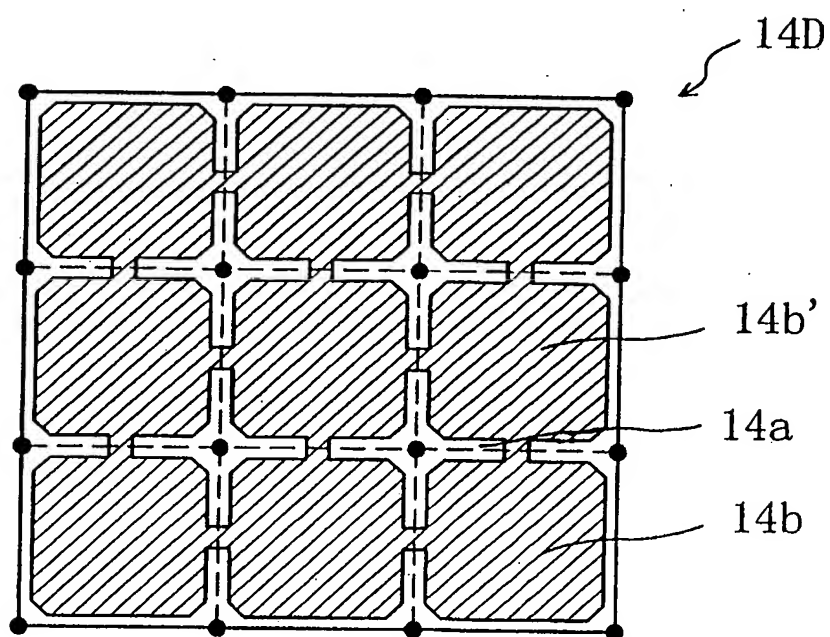
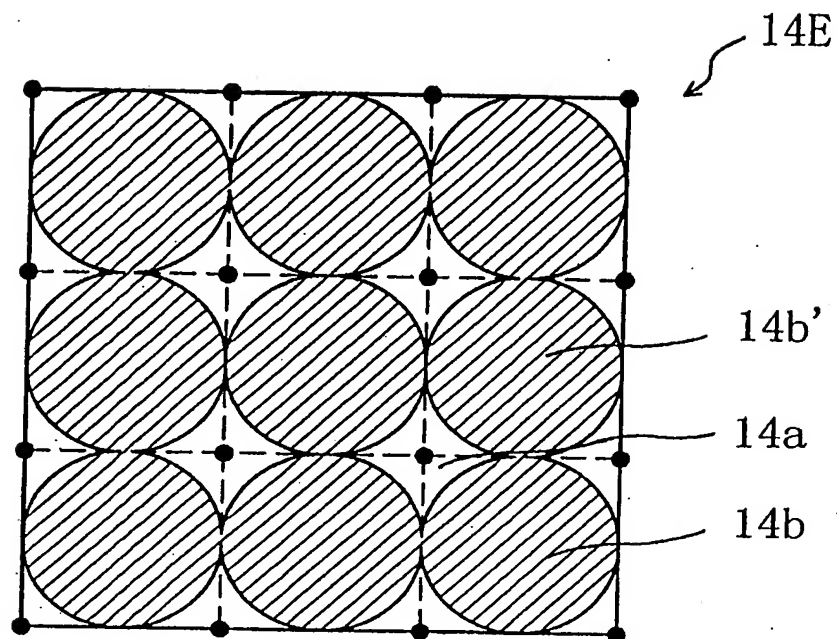


FIG. 8

(a)



(b)

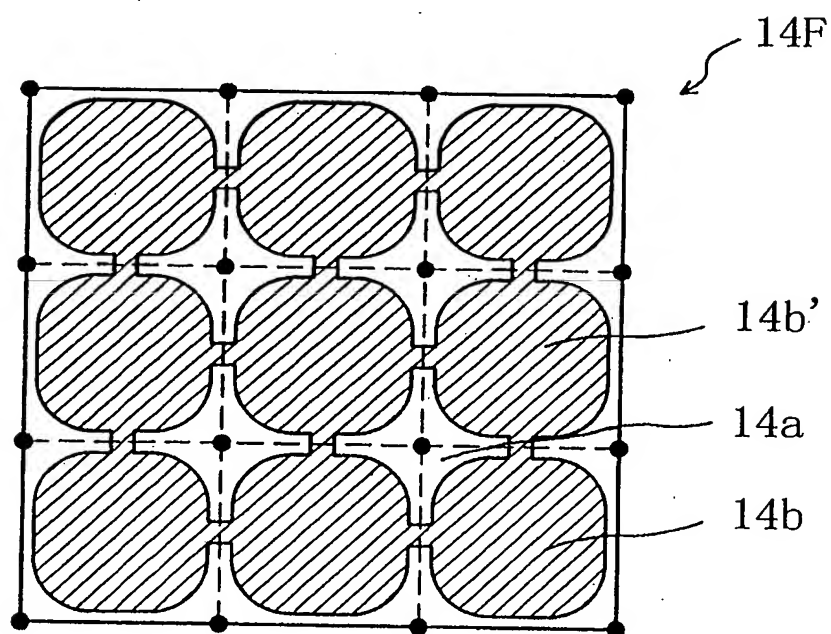


FIG. 9

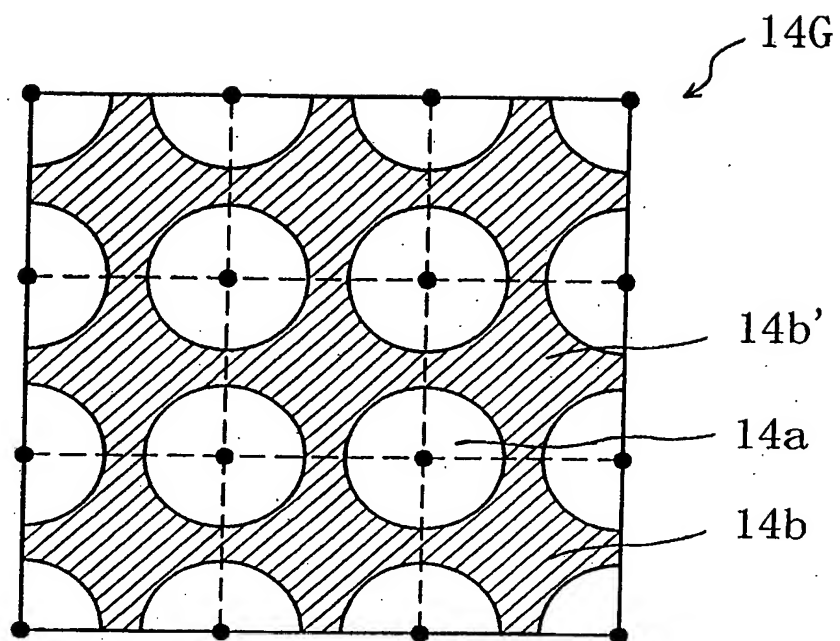
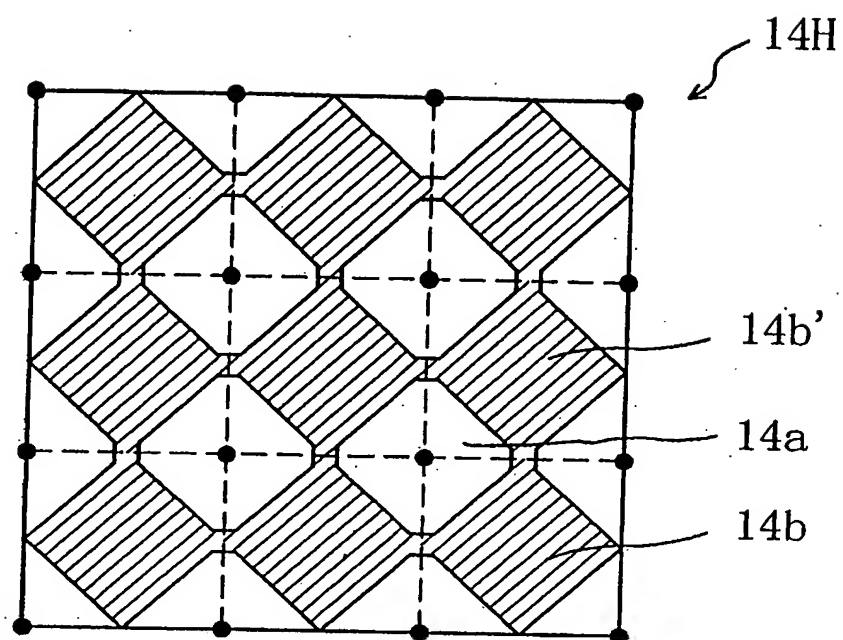


FIG. 10

(a)



(b)

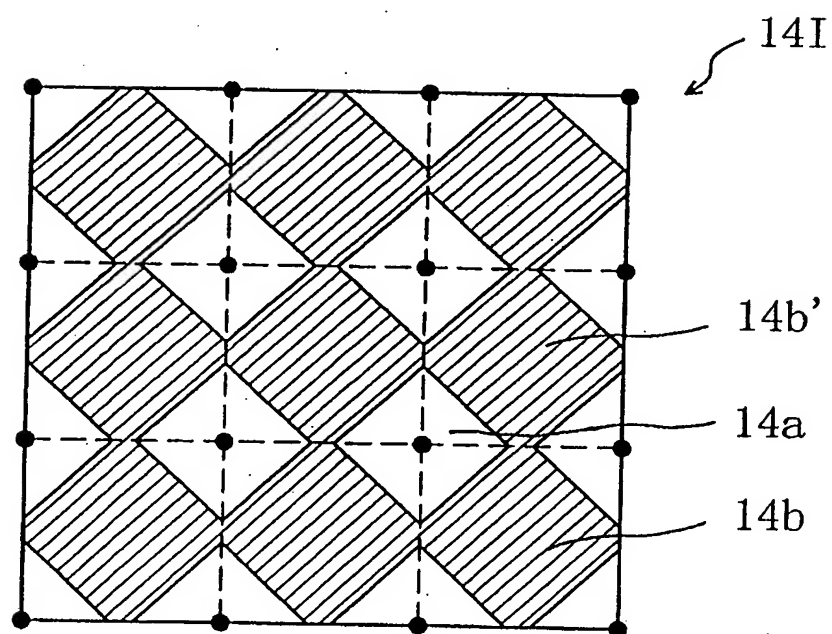
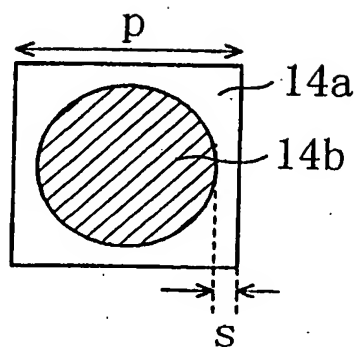
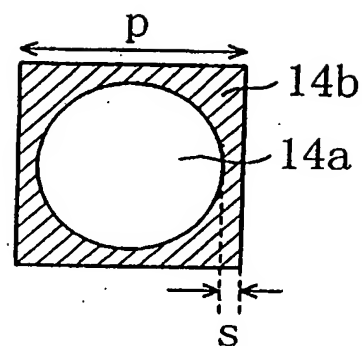


FIG. 11

(a)



(b)



(c)

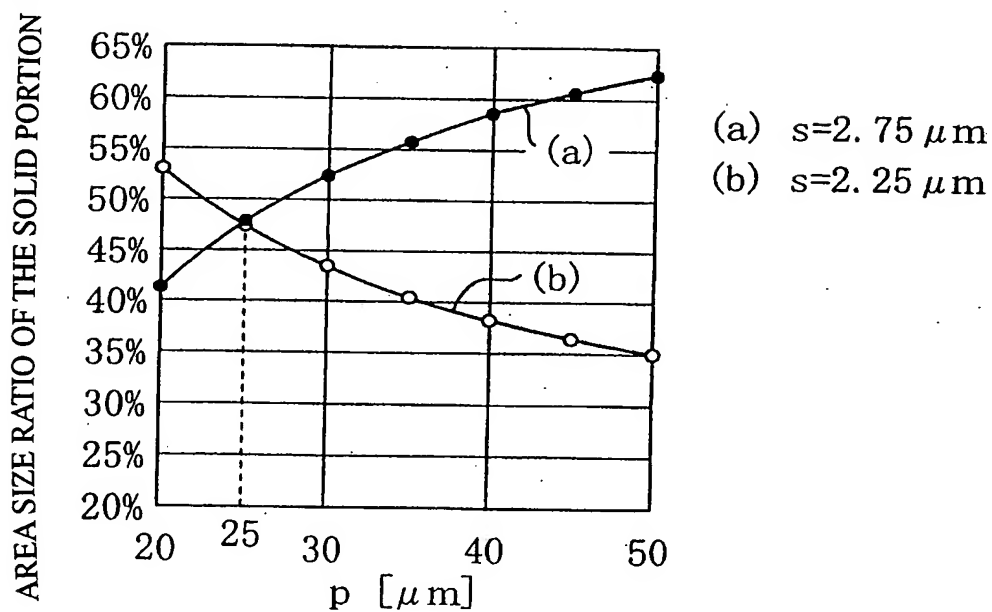
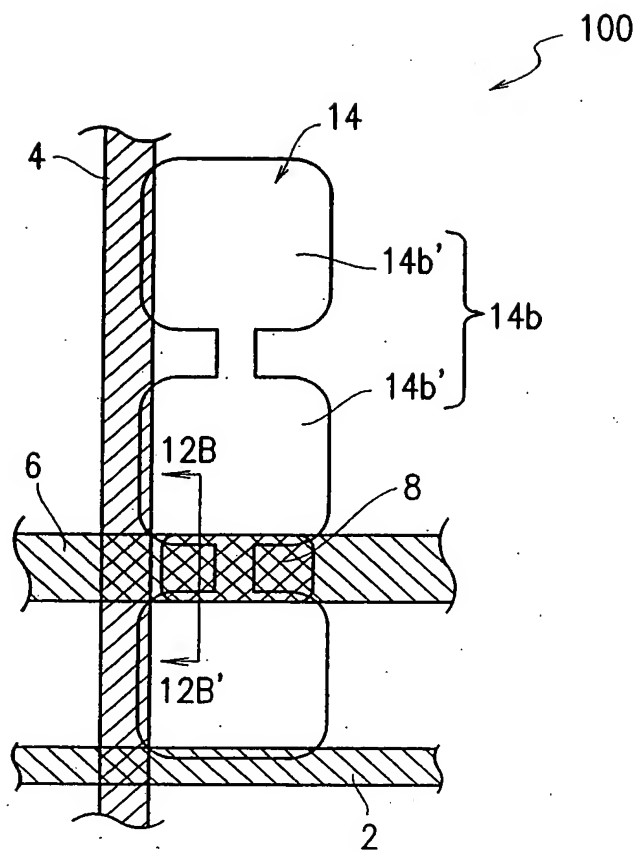


FIG. 12

(a)



(b)

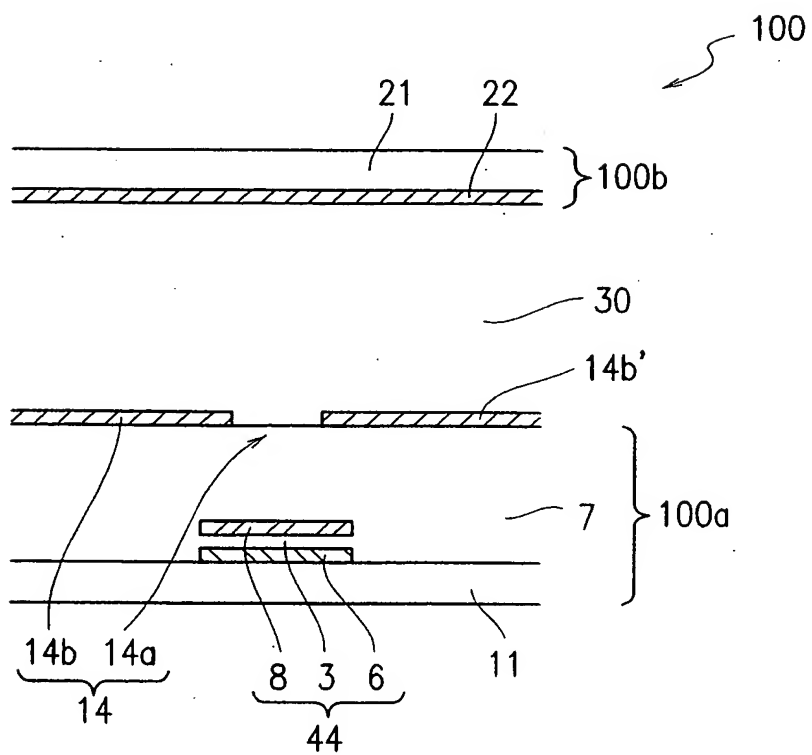


FIG. 13

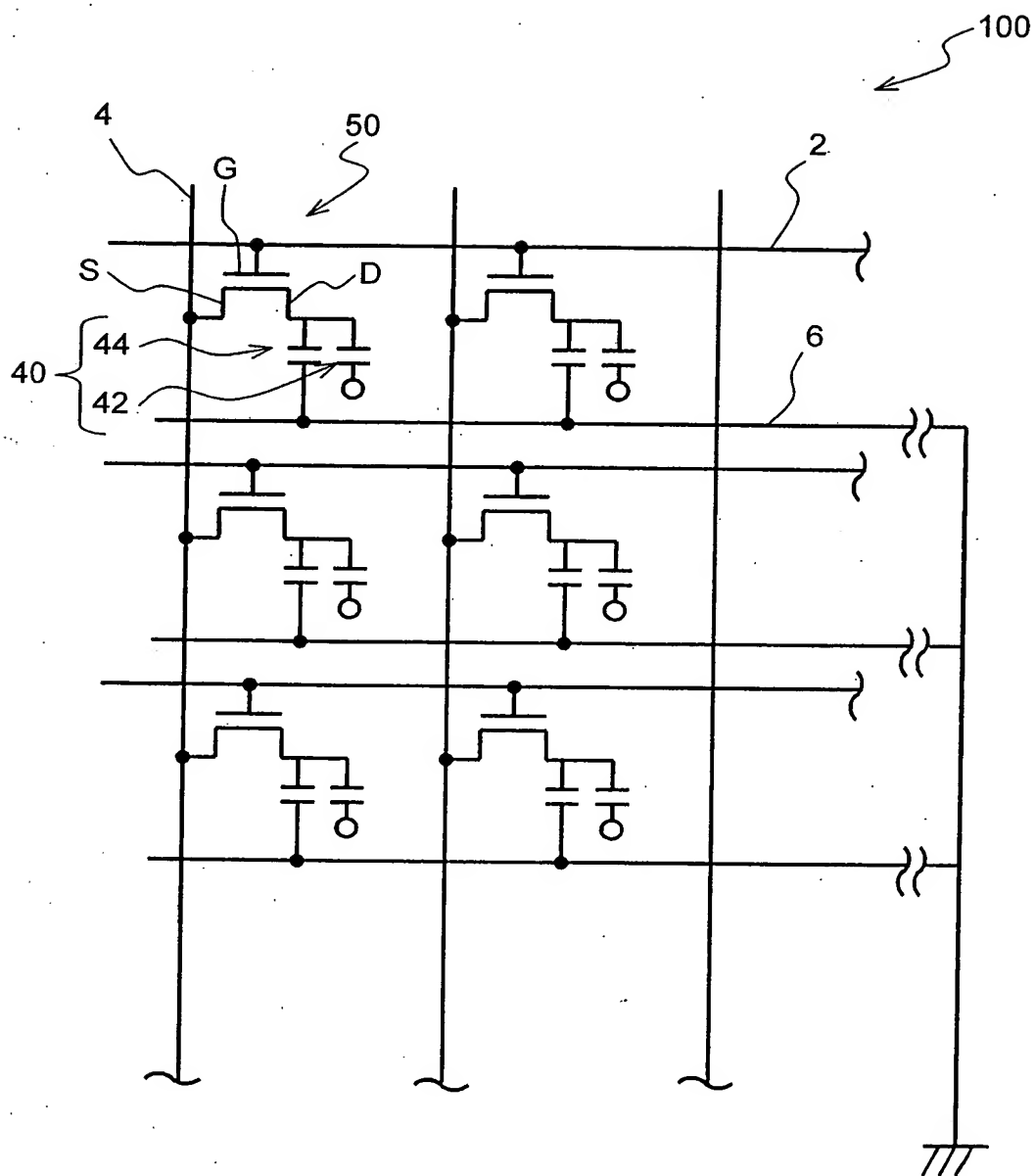


FIG. 14

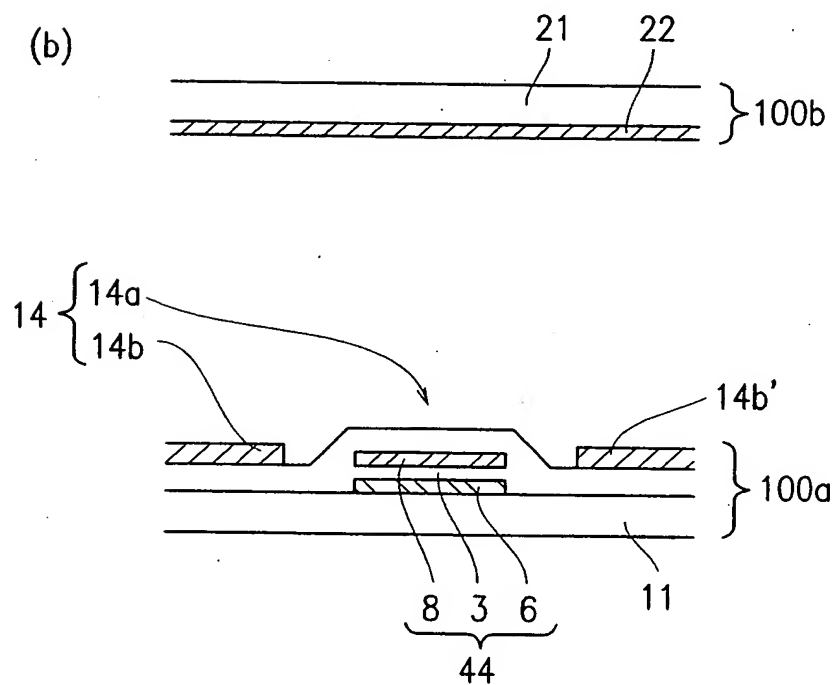
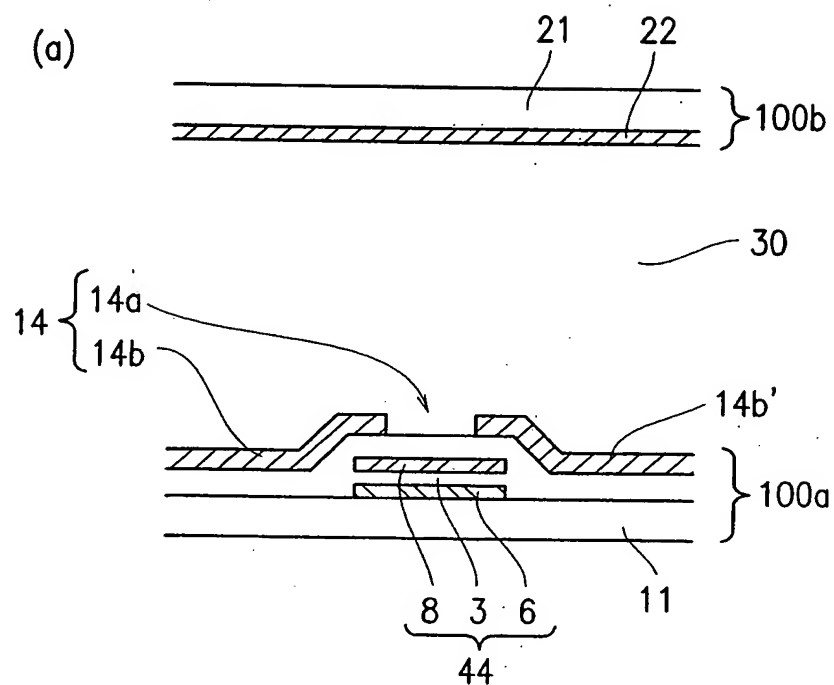
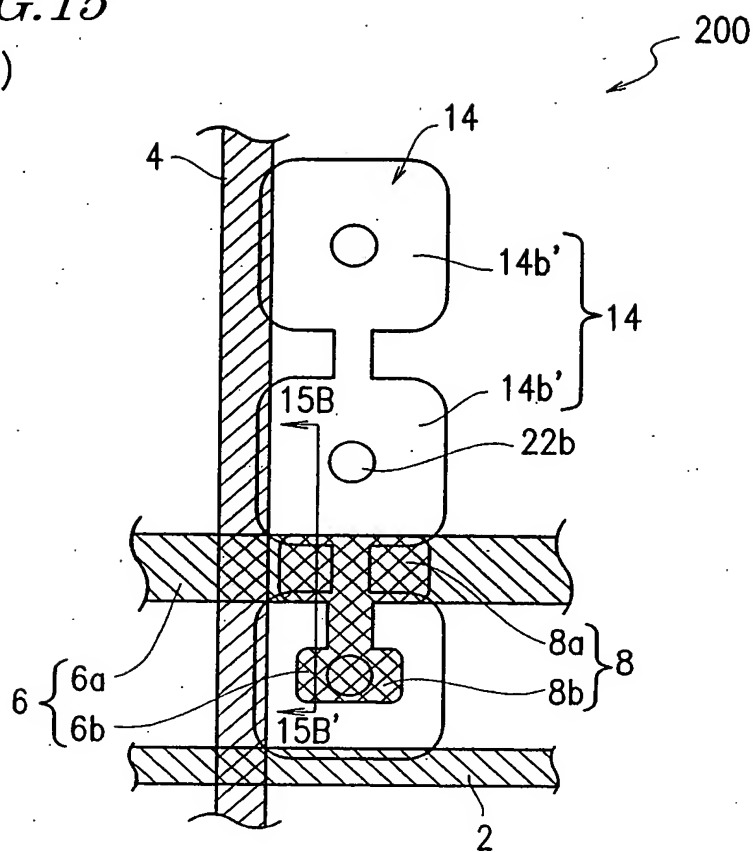


FIG. 15

(a)



(b)

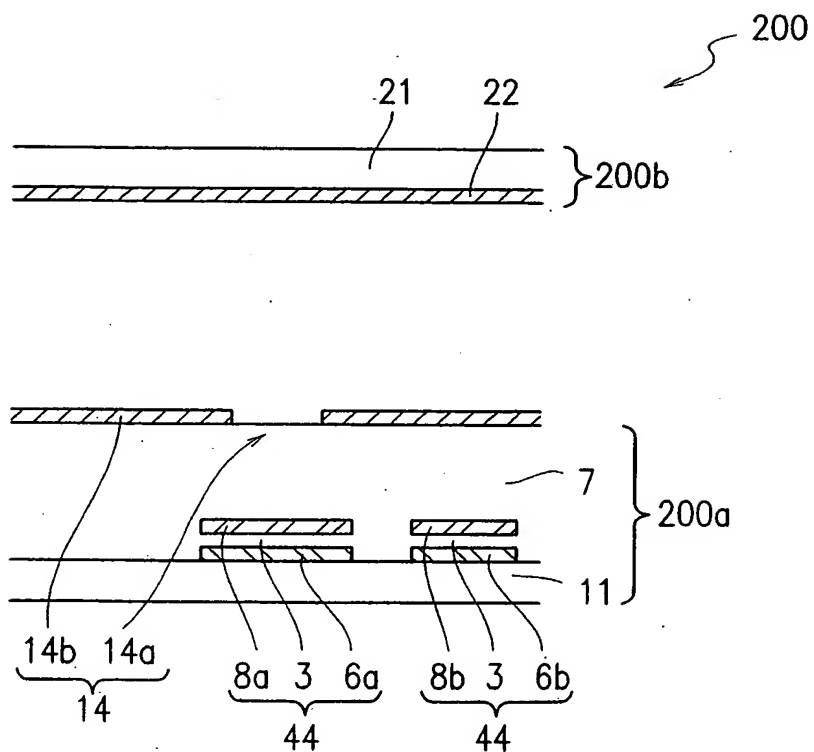


FIG. 16

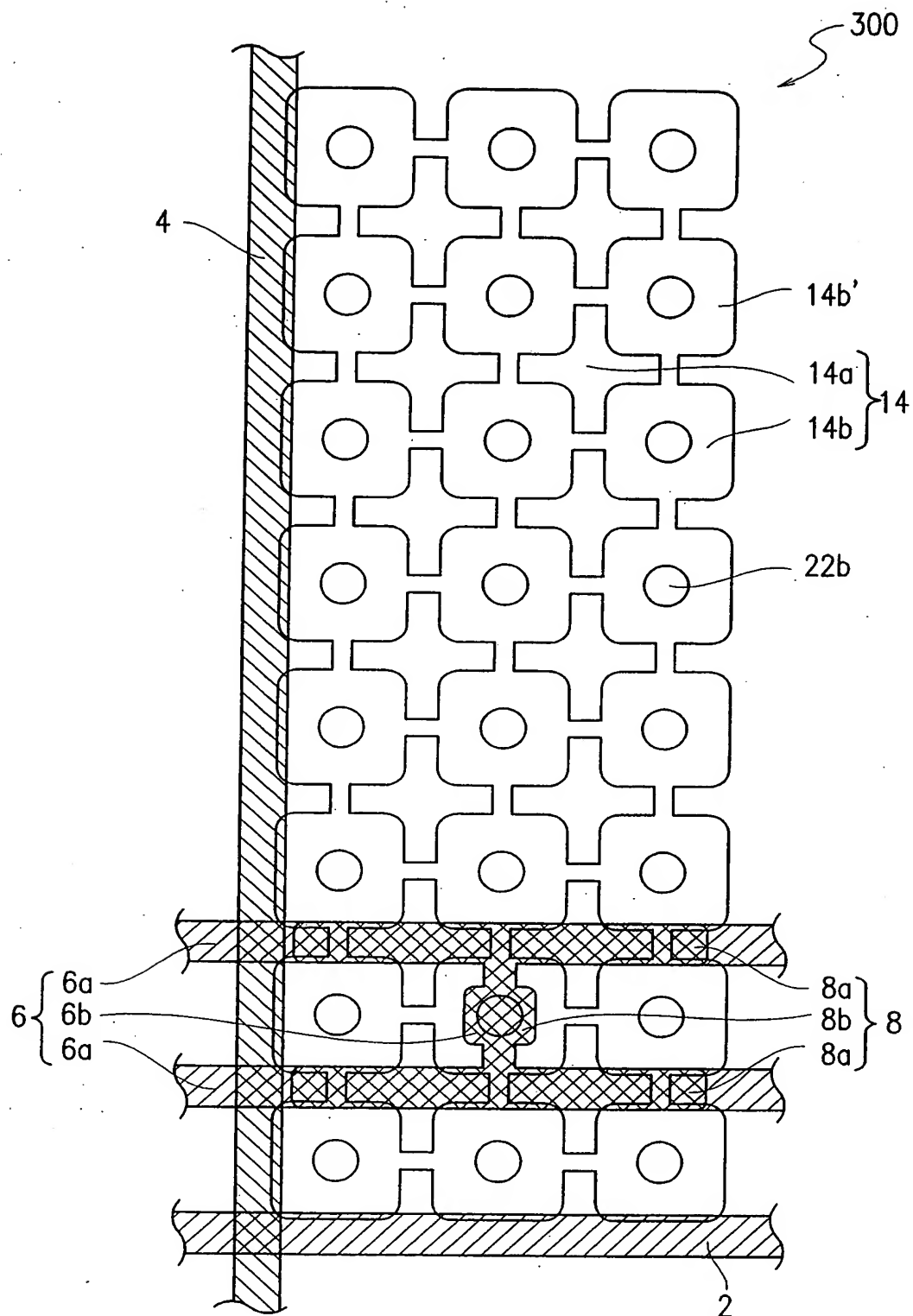


FIG. 17

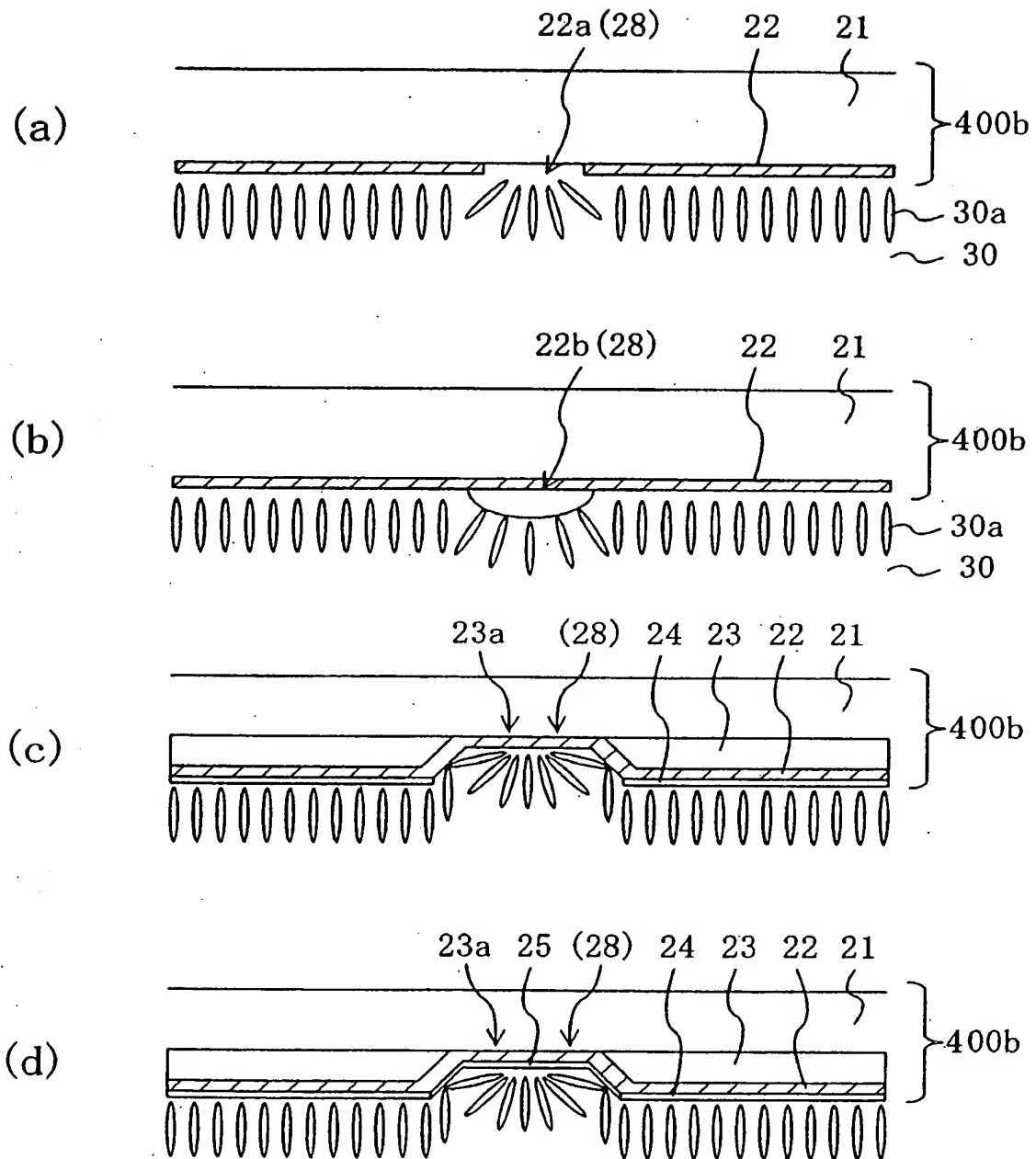


FIG. 18

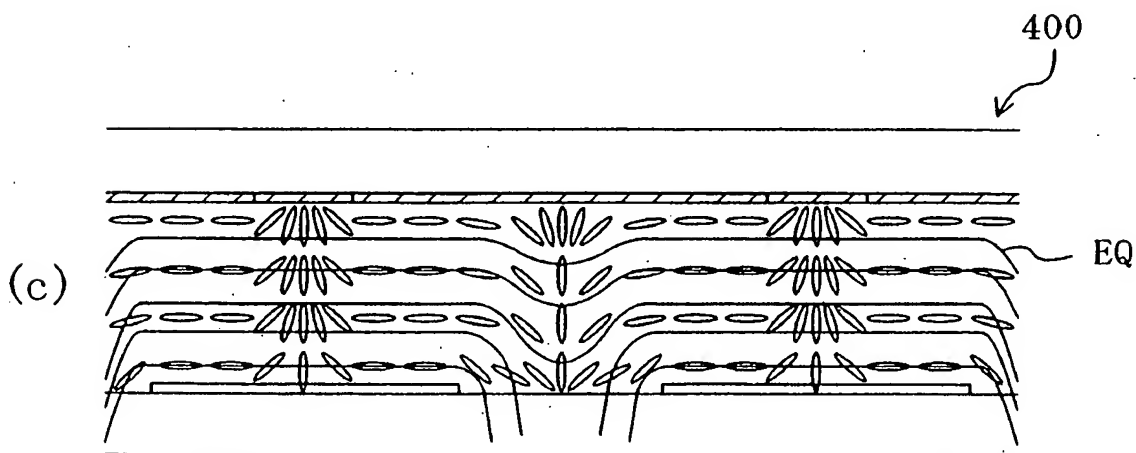
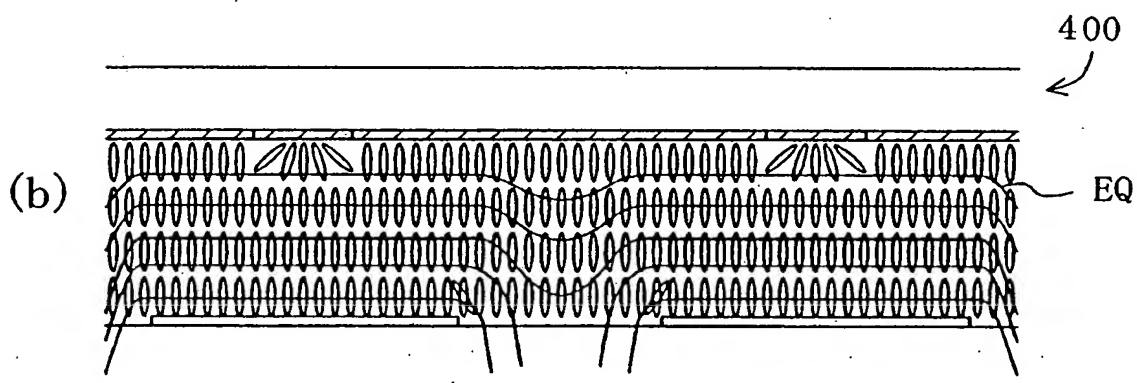
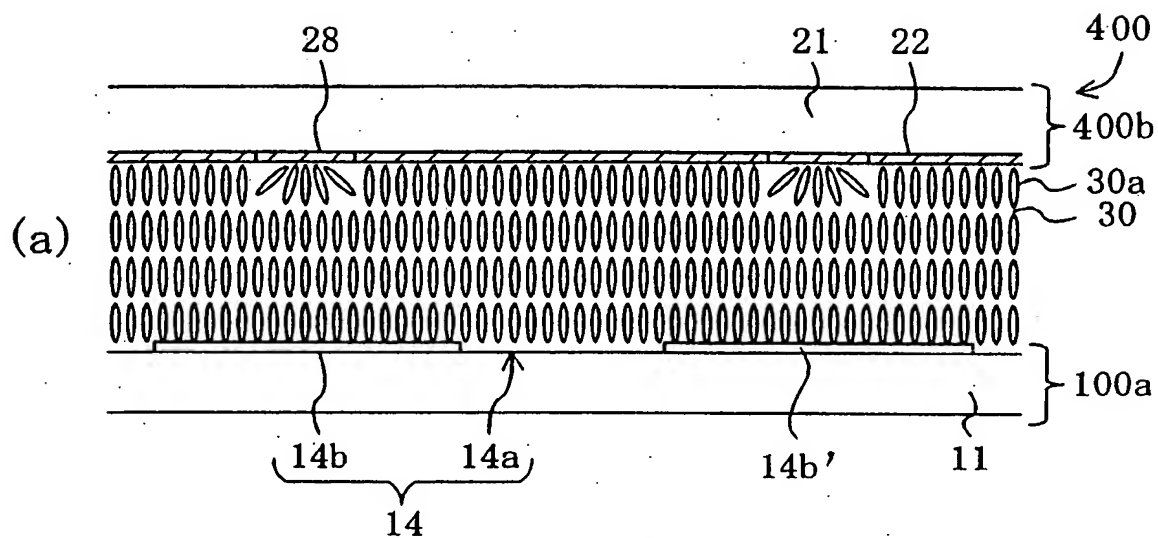


FIG. 19

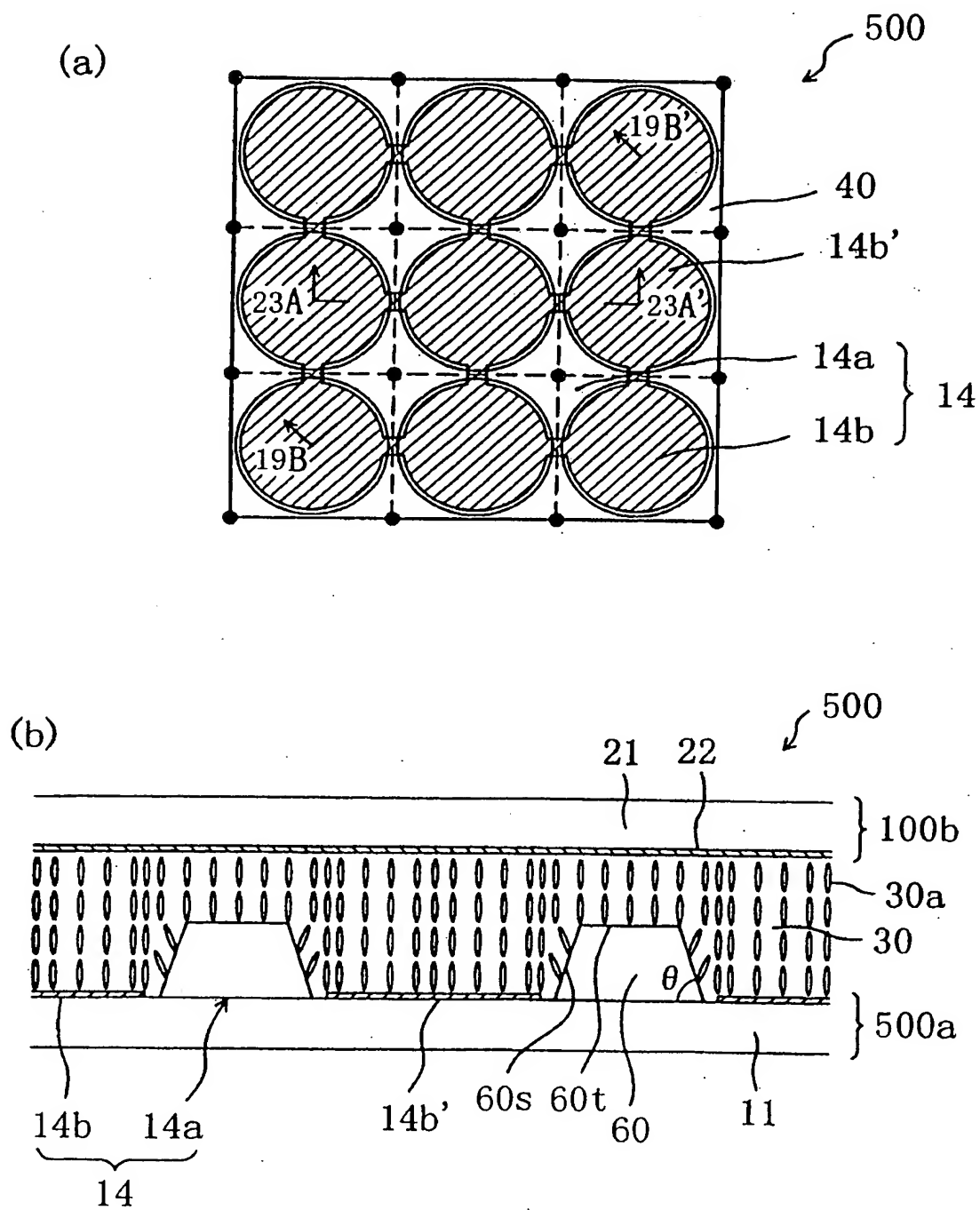


FIG. 20

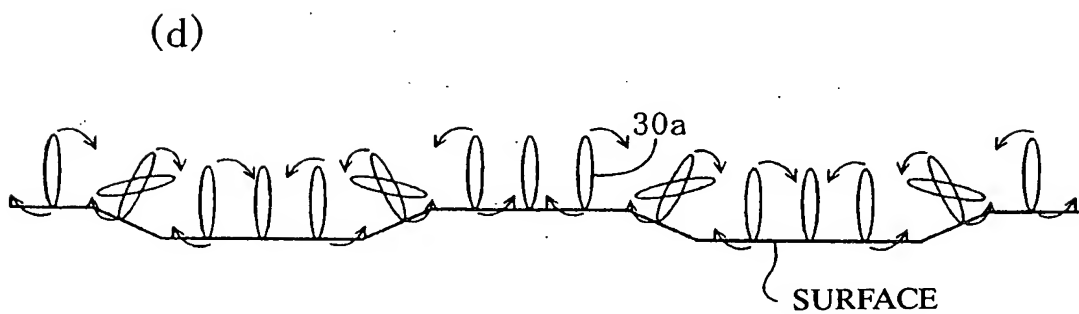
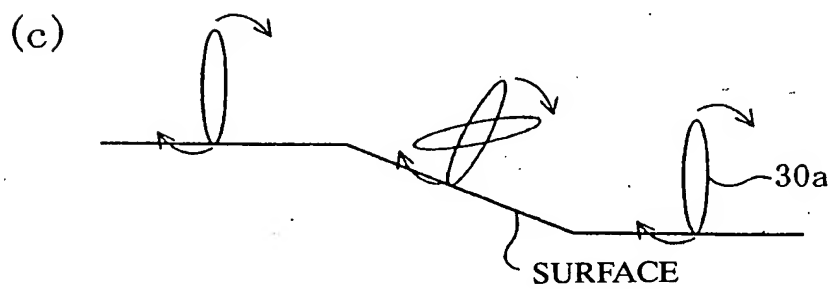
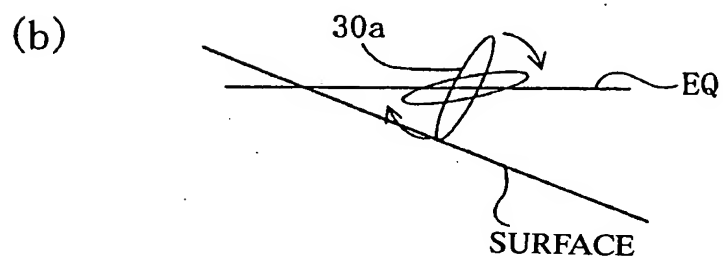
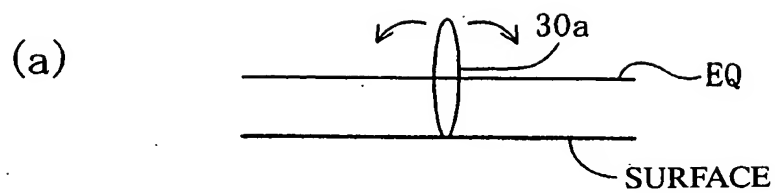


FIG. 21

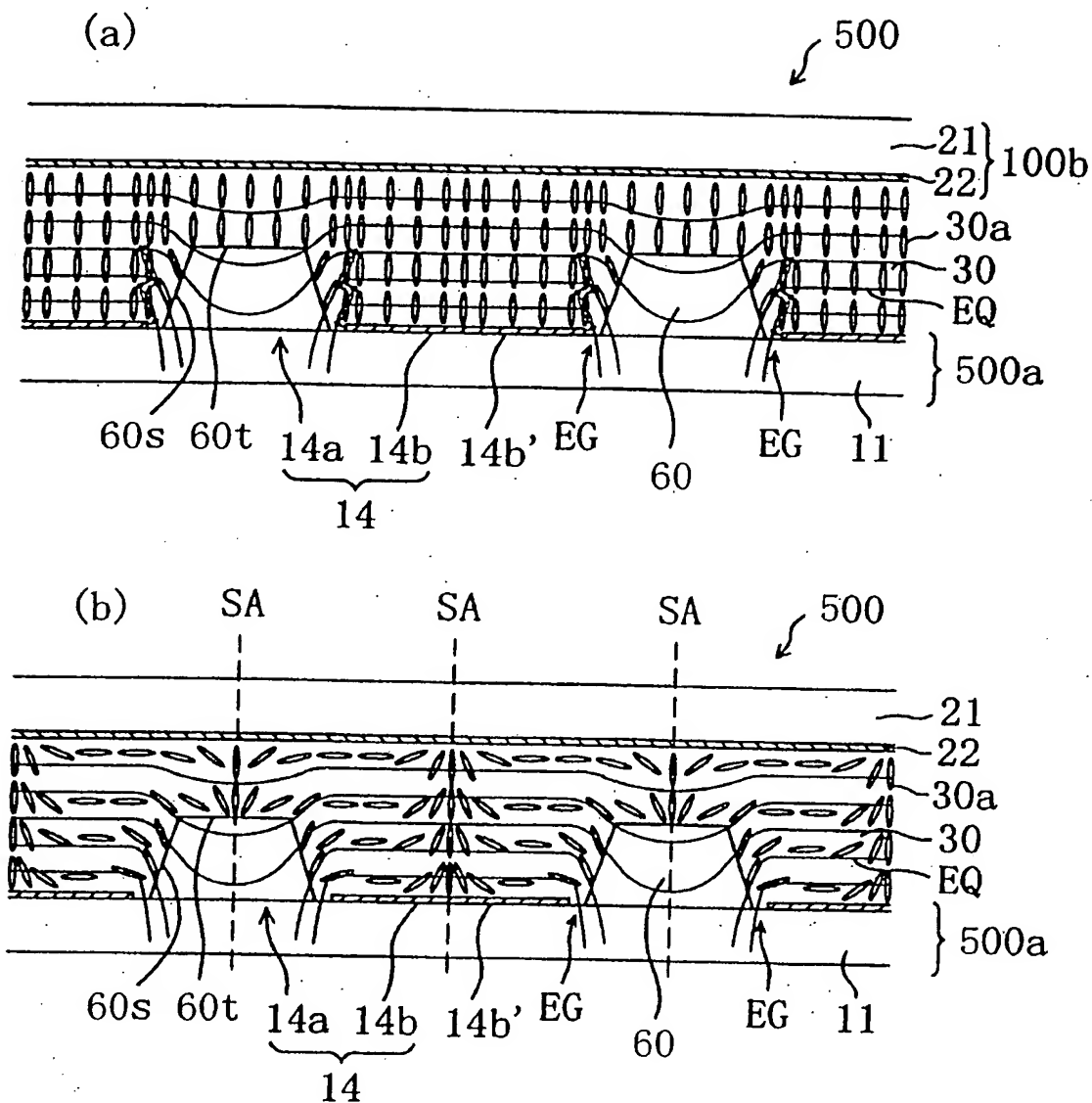


Fig. 1 consists of three cross-sectional views of a semiconductor device, labeled (a), (b), and (c). Each view shows a substrate with a series of horizontal lines representing different layers. In (a), the device is in a state before etching, with a central region labeled 100b. In (b), the device is in a state after etching, with a central region labeled 100a. In (c), the device is in a state after etching and annealing, with a central region labeled 100c. The views show the formation of a central region (100a, 100b, 100c) and the surrounding regions (14a, 14b, 60A, 60B, 60C, 60s). The layers are labeled EQ, 30a, and 500a. The views are labeled 500A, 500B, and 500C.

FIG. 23

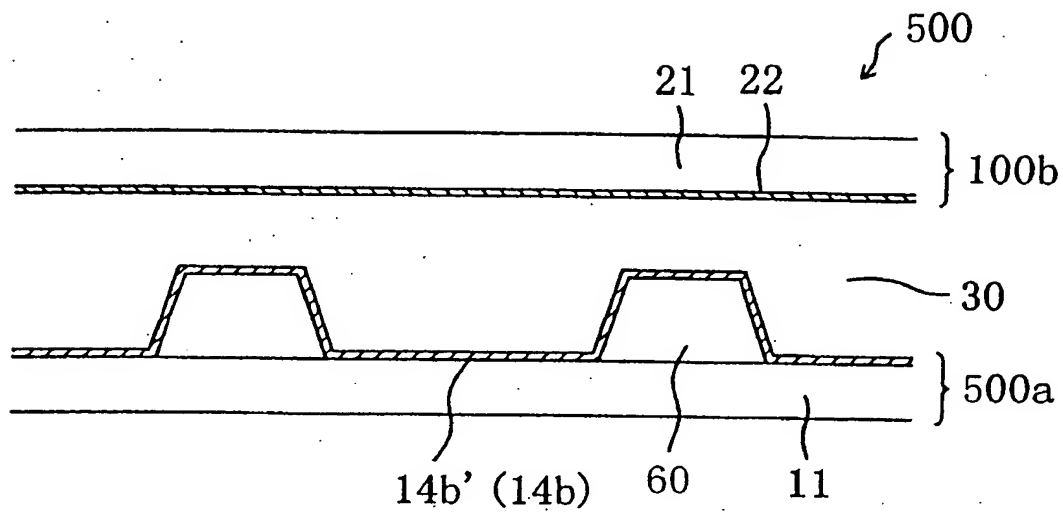


FIG. 24

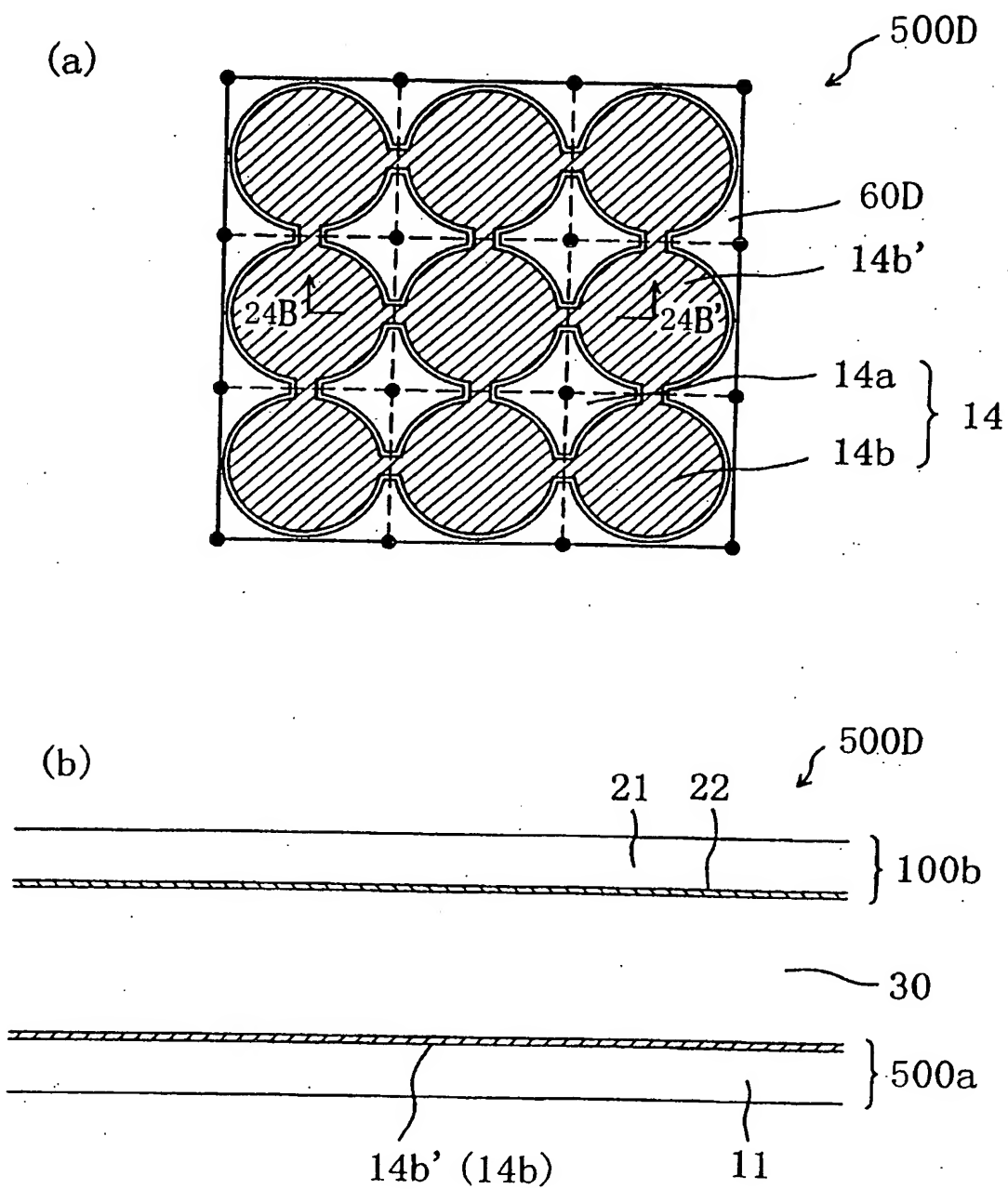


FIG. 25

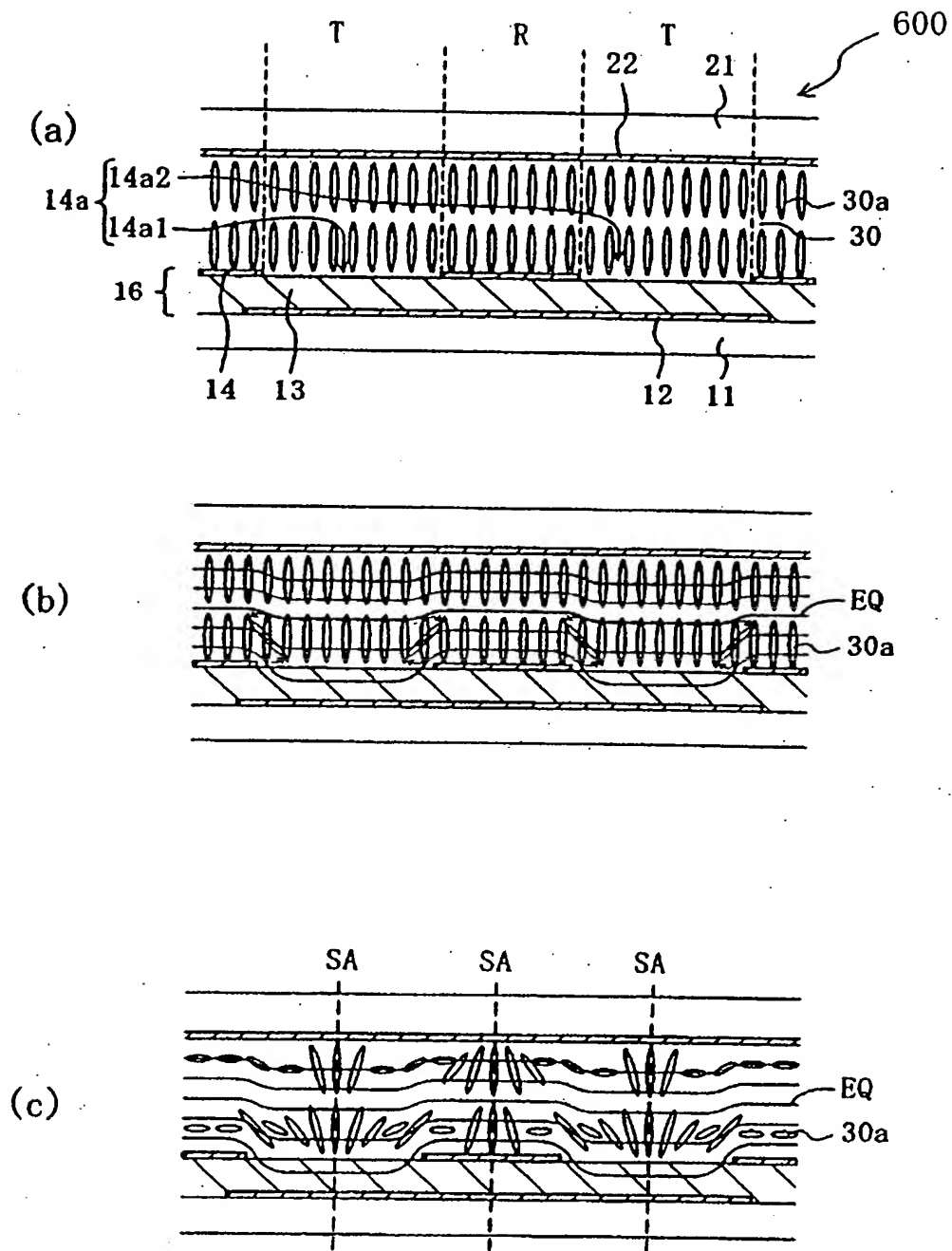


FIG. 26

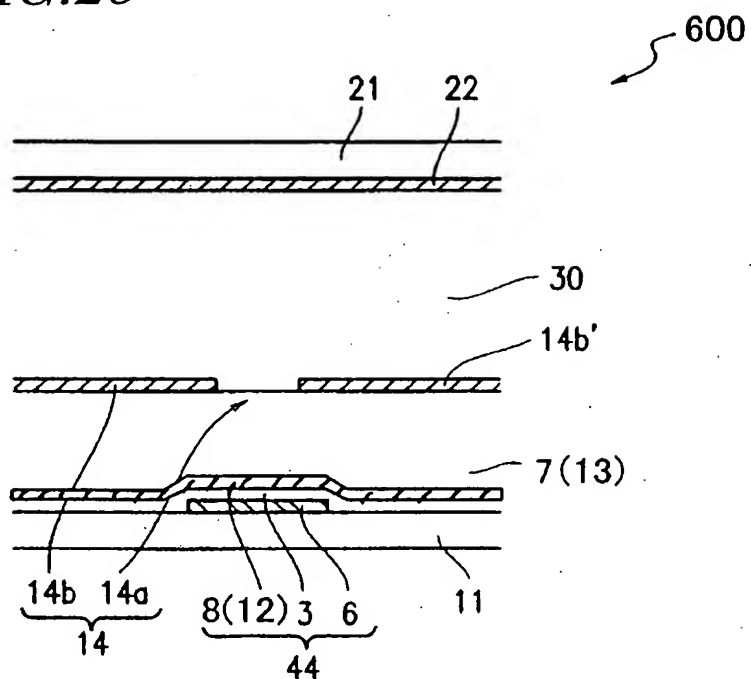


FIG. 27

